AMENDMENTS TO THE CLAIMS

The claims and their status are reflected below. Claims 1-12 and 18-23 are pending in the application.

1. (currently amended) A method of making an array of non-volatile memory cells on a semiconductor substrate surface, comprising:

forming an array of first floating gate portions across the substrate surface with a gate dielectric layer therebetween,

subsequently forming a masking layer over areas of the substrate not covered by first floating gate portions such that a pattern of openings in the masking layer is self-aligned to the first floating gate portions,

forming sidewall elements in the openings in the masking layer over first floating gate portions,

forming second floating gate portions defined by the sidewall elements in at least one direction and contacting the first floating gate portion, and

subsequently removing the sidewall elements thereby exposing surfaces of the first and second floating gate portions.

2. (original) The method of claim 1, wherein the first floating gate portions are formed by depositing a layer of gate material, thereafter depositing a layer of dielectric material over the gate material, thereafter etching the dielectric material and gate material in the same pattern to form structures comprising first floating gate portions covered by dielectric material.

3. (original) The method of claim 2 further comprising implanting impurities into the substrate while first floating gate portions covered by dielectric material are present so as to implant impurities only in the areas of the substrate not covered by floating gate portions covered by dielectric material.

4. (original) The method of claim 2, wherein the masking layer is formed by depositing masking layer material over the surface of the substrate and thereafter removing masking layer material that overlies first floating gate portions covered by dielectric material.

5. (original) The method of claim 4, wherein the dielectric material is removed after the masking layer material that overlies first floating gate portions covered by dielectric material is removed.

6. (original) The method of claim 1, wherein the sidewall portions are formed by deposition and etch back of silicon nitride.

7. (original) The method of claim 1, wherein the second floating gate portion is formed by deposition and etch back of polysilicon.

8. (currently amended) The method of claim 1, further comprising:
~~removing the sidewall elements thereby exposing surfaces of the first and second floating gate portions,~~
forming a dielectric layer on the exposed floating gate portion surfaces, and
forming conductive gates extending across the floating gates in at least one direction and in contact with the dielectric layer.

9. (original) The method of claim 8, wherein the dielectric layer is an ONO layer.

10. (original) The method of claim 8, wherein the conductive gates extend towards the surface of the semiconductor substrate such that the lowest extremities of the conductive gates are closer to the surface of the semiconductor substrate than the highest extremities of the second floating gate portions.

11. (original) The method of claim 10 wherein the conductive gates extend to enclose the second floating gate portions from above and on four lateral sides.

12. (original) The method of claim 8 further comprising the step of depositing a metal on the conductive polysilicon gates and exposing to increased temperature to produce a silicide layer.

13.-17. (canceled)

18. (currently amended) A method of making an array of non-volatile memory cells on a semiconductor substrate surface, comprising:

forming an array of first floating gate portions, wherein each first floating gate portion is physically separated from adjacent first floating gate portions,

thereafter forming second floating gate portions extending from first floating gate portions, wherein ~~each~~ an individual second floating gate portion extends along a plane perpendicular to the plane of the substrate surface and wherein the plane of the second floating gate portion bisects the first floating gate portion, the second floating gate portion being self-aligned to the first floating gate portion.

19. (original) The method of claim 18 wherein the first floating gate portions are square in shape and the second portions extend from a line that is approximately a midline of the square.

20. (previously presented) A method of forming a non-volatile memory array on a substrate surface, comprising:

forming a layer of gate dielectric material extending across the substrate surface,

forming a layer of floating gate material extending across the layer of gate dielectric material and in contact with the layer of gate dielectric material,

subsequently forming shallow trench isolation structures that divide the layer of floating gate material into strips of floating gate material that extend in a first direction,

subsequently forming a first masking layer that extends over the shallow trench isolation structures and strips of floating gate material,

forming a plurality of first masking strips from the first masking layer, the plurality of first masking strips extending in a second direction that is perpendicular to the first direction,

forming a plurality of physically separate first floating gate portions by removing portions of strips of floating gate material that are not covered by the plurality of first masking strips,

subsequently forming a plurality of second masking strips that fill spaces between the plurality of first masking strips, second masking strips extending in the second direction,

subsequently removing the plurality of first masking strips,

forming spacers along sidewalls of the plurality of second masking strips, the spacers overlying the first floating gate portions, and

subsequently forming second floating gate portions by filling gaps between spacers of adjacent second masking strips.

21. (previously presented) The method of claim 20 further comprising forming source and drain areas by implanting subsequent to forming the plurality of physically separate first floating gate portions, using the plurality of first masking strips to define implanted regions.

22. (previously presented) The method of claim 20 further comprising, subsequent to forming second floating gate portions, removing spacers and depositing a layer of dielectric over first and second floating gate portions.

23. (previously presented) The method of claim 21 further comprising forming a plurality of control gates extending in the second direction, a control gate extending between second masking strips, over the layer of dielectric, to surround a second floating gate portion from four lateral sides.